

RF POWER AMPLIFIER

1300 MHz Power Amplifier for Amateur Radio Applications

- Design goals
 - Brief Power Amplifier Theory
 - Load-Pull and source pull simulation results
 - Matching Networks
 - Small signal simulation results
 - Large signal
 - Stability of the power amplifier
 - layout
 - Conclusion
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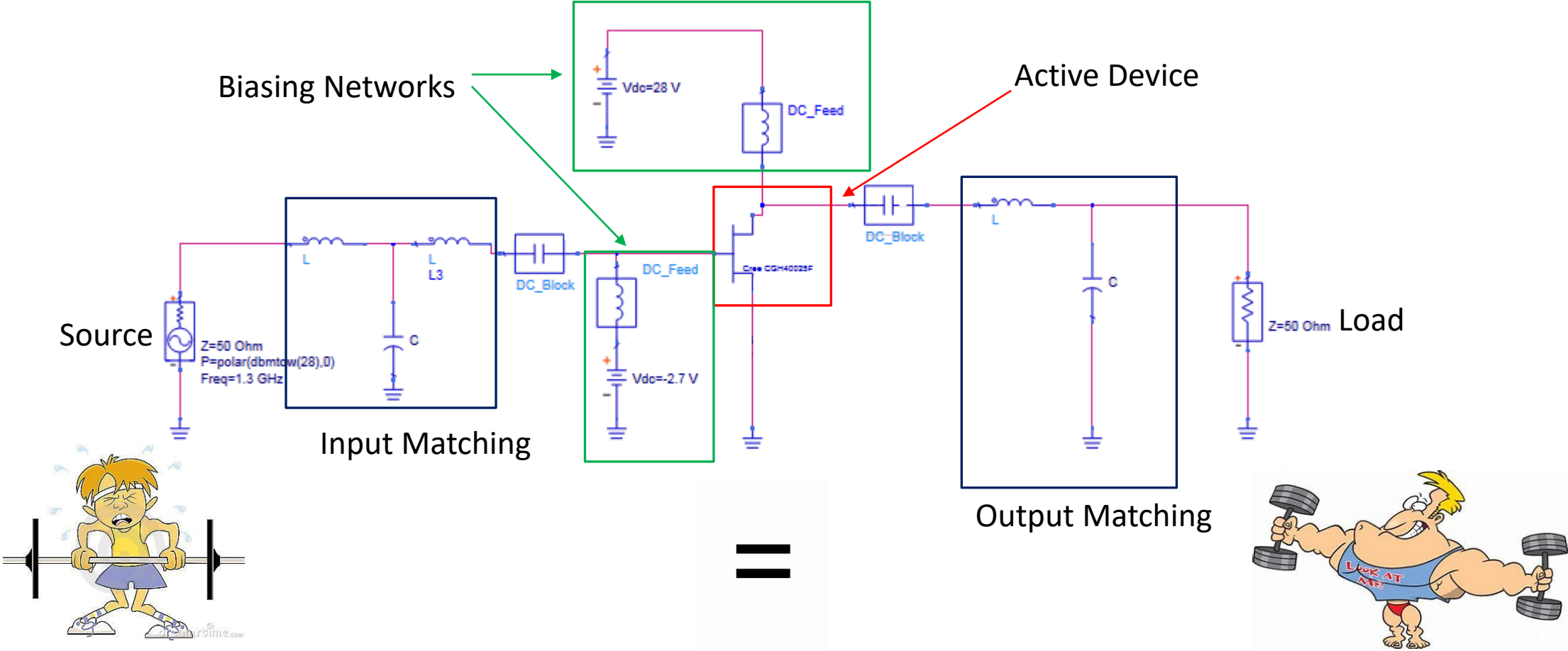
AIM



Design goals

- Operating Frequency of 1300 MHz
- Gain of 15dB
- Output Power 25W
- Narrow band (85MHz)
- Efficiency of 50% plus

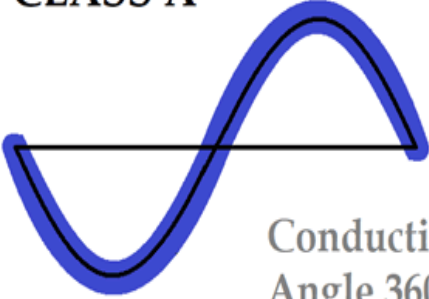
Power Amplifier Theory and Circuit Design



Power Amplifier Classes

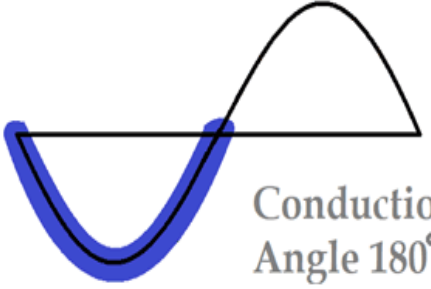
Classes	A	B	AB
Efficiency %	50	80	50 - 70
Conduction Angle (degrees)	360	180	180 - 200
Gain	Higher	Lower	Higher than B but lower than A

CLASS A



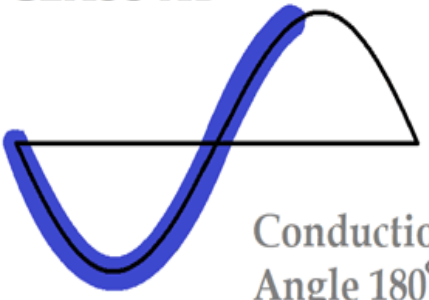
Conduction Angle 360°

CLASS B



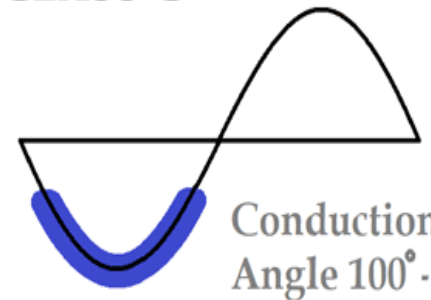
Conduction Angle 180°

CLASS AB



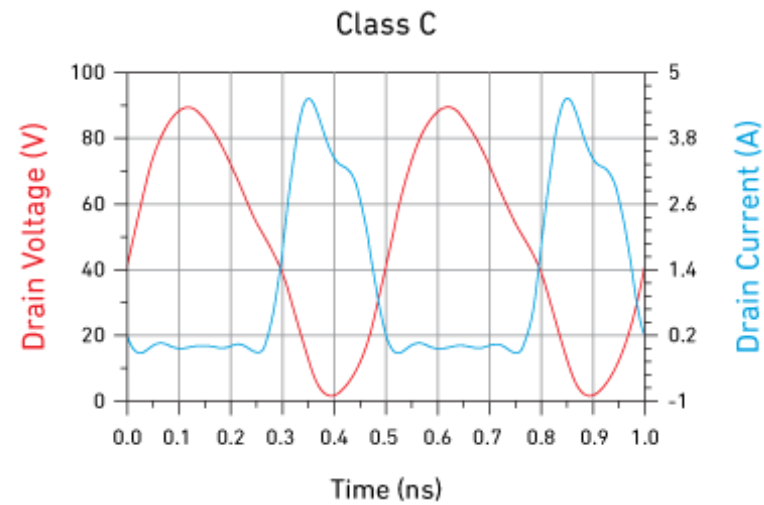
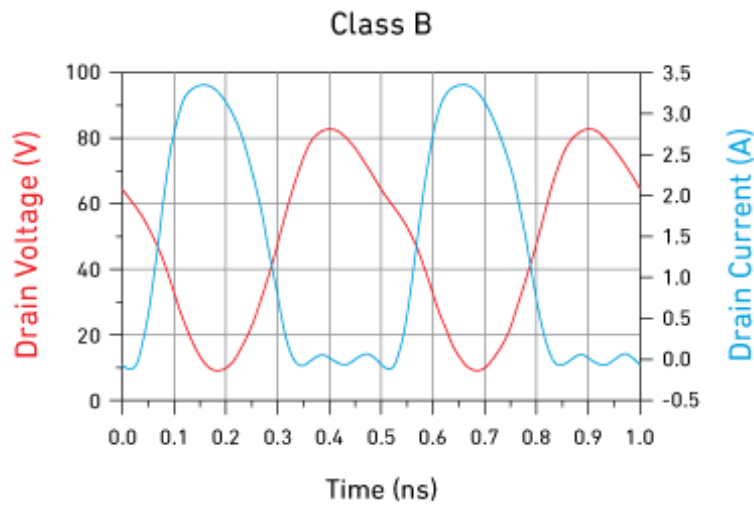
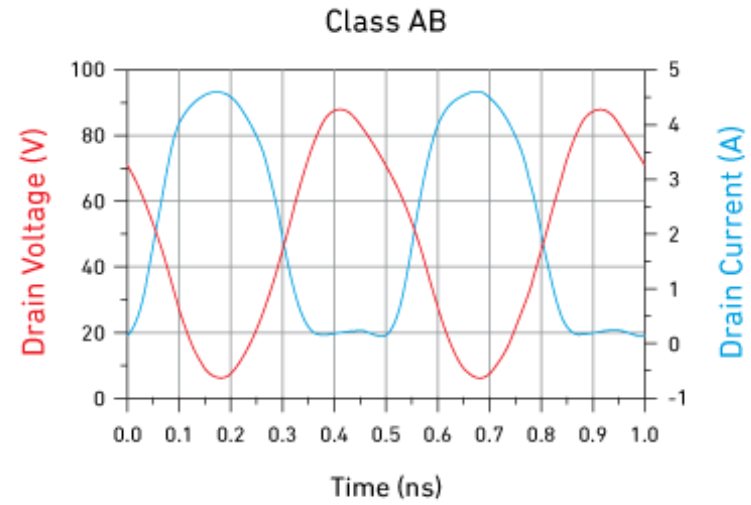
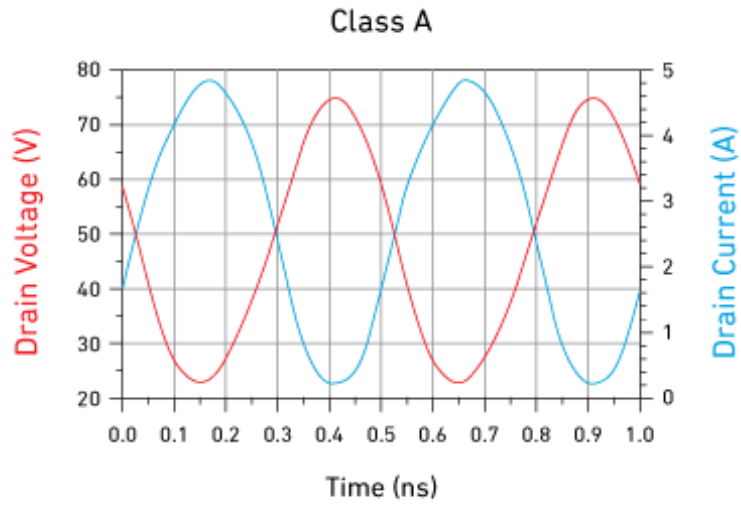
Conduction Angle $180^\circ - 200^\circ$

CLASS C



Conduction Angle $100^\circ - 150^\circ$

I-V Waveforms at Intrinsic Nodes to Illustrate Basic PA Classes

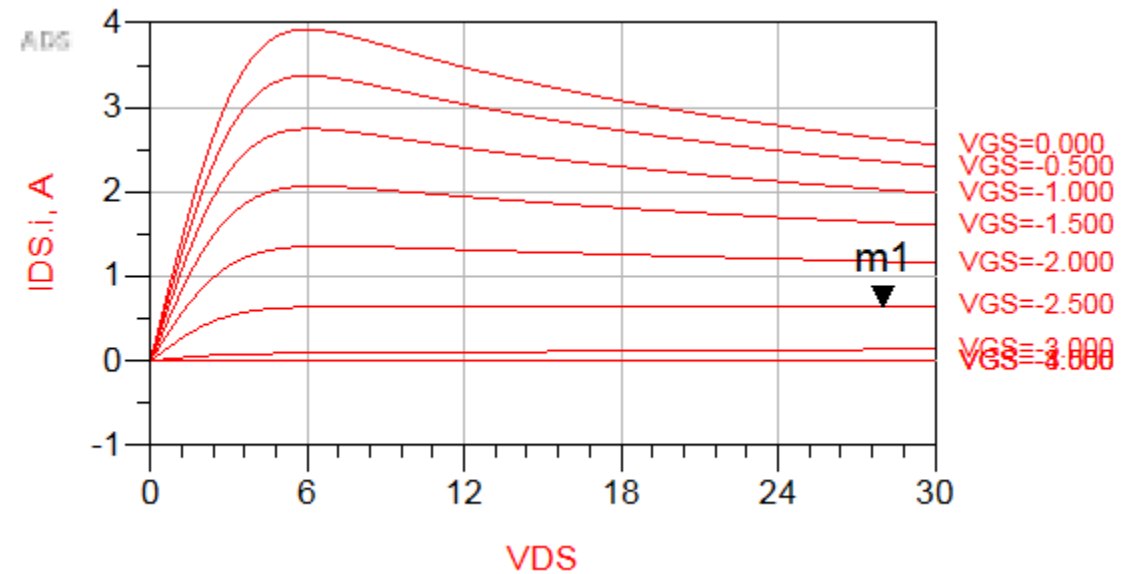


Characterising the device

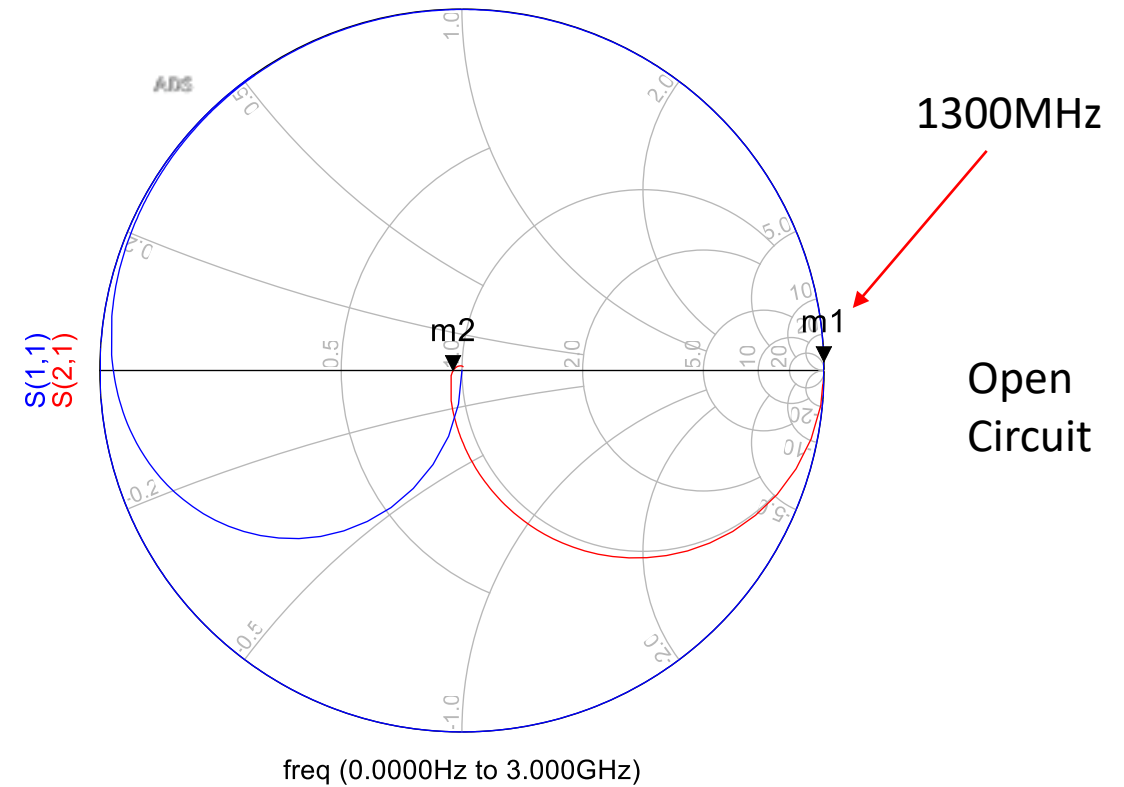
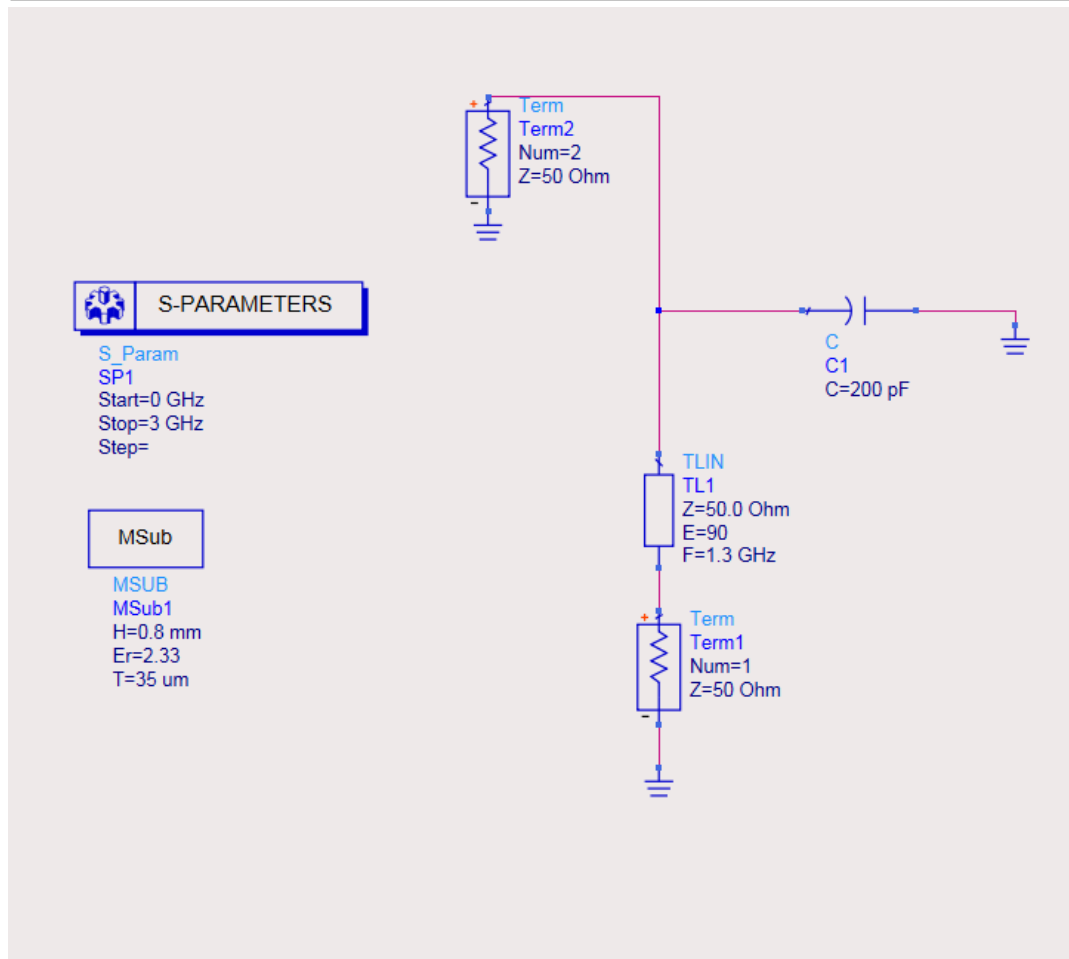
25W GaN CGH40025F 25W

Device Specifications

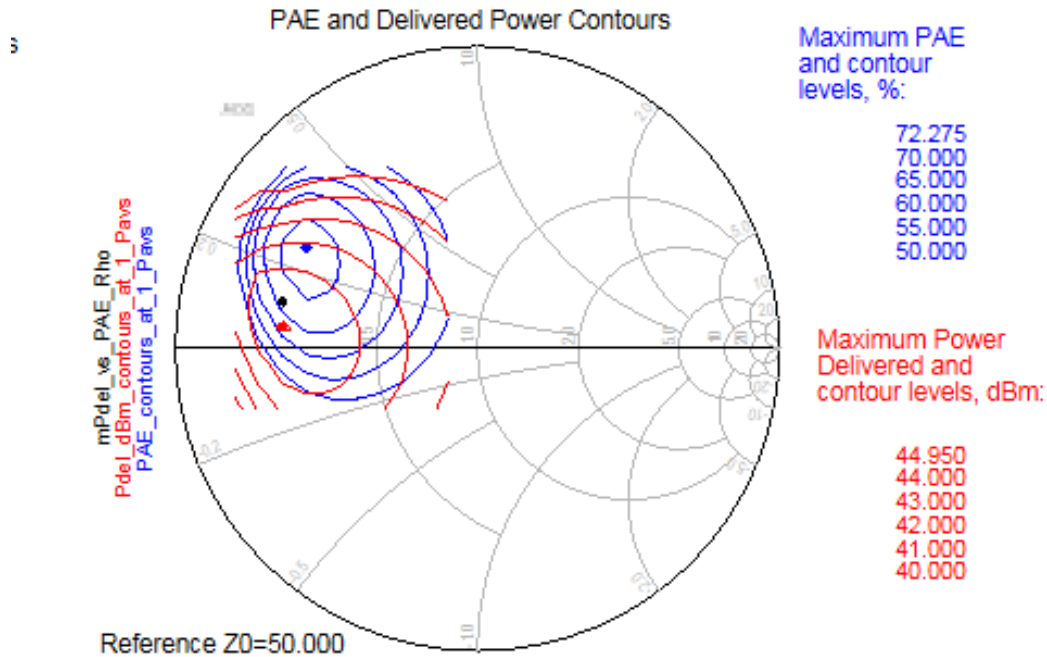
- ✓ Operating voltage of 28 V
- ✓ High Power tolerance
- ✓ Operating frequency up 6 GHz
- ✓ Easy to match to



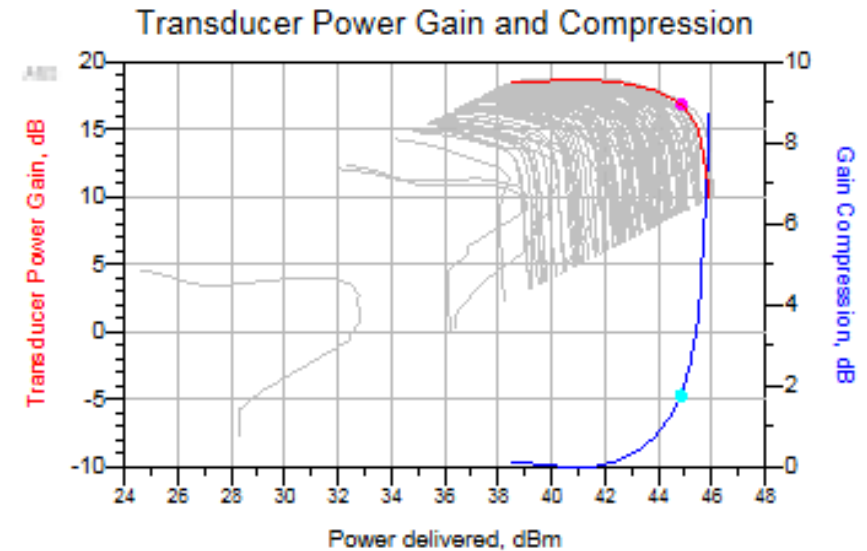
Biasing Networks



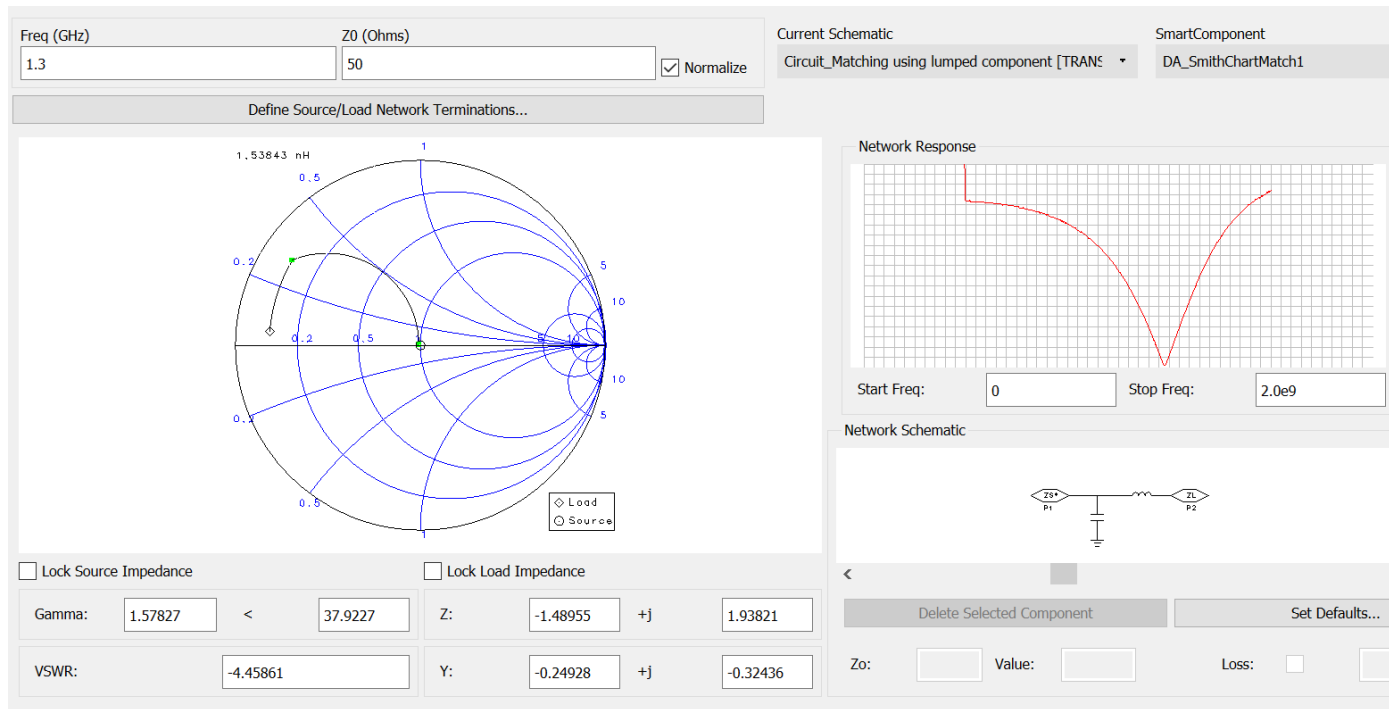
Load-Pull Simulation



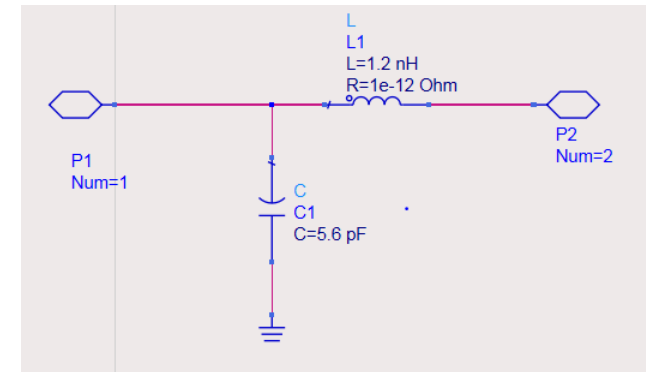
Input impedance	$Z_s = 0.646 - j1.761 \Omega$
Output impedance	$Z_L = 10.27 + j5.7 \Omega$
Efficiency	67%
Gain	15 dB



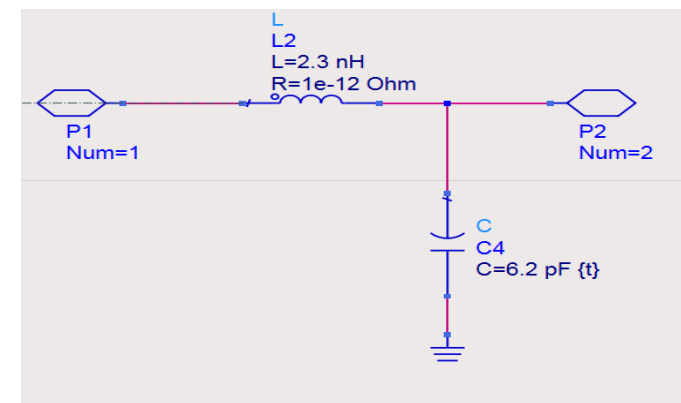
Matching Networks



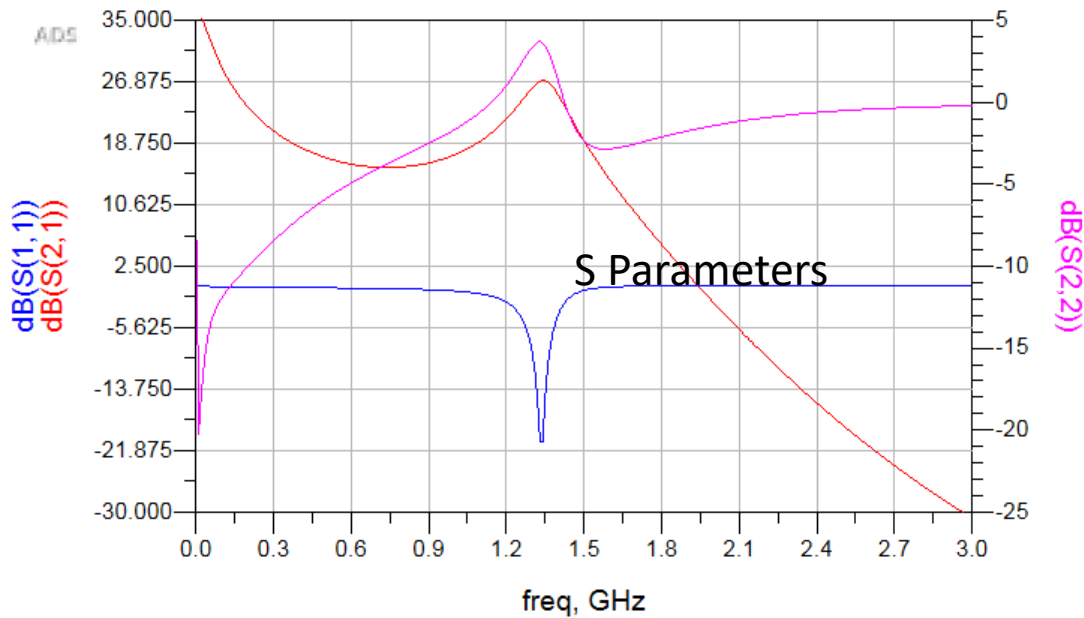
Input Matching network



Output Matching network



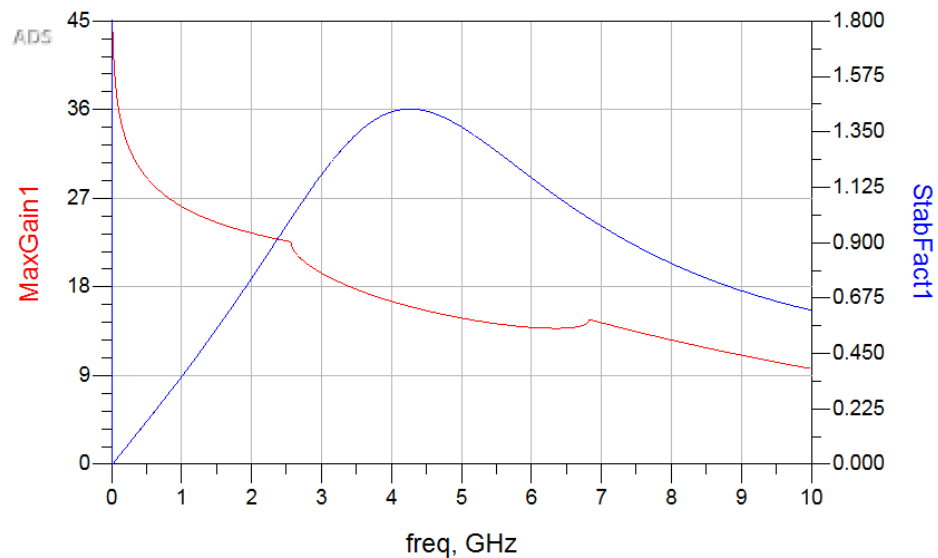
S -Parameter



S Parameters	Value @ 1.3GHz (dB)
S 2,1	27+
S 1,1	-20.7
S 2,2	3.6

Stability (Without stability network)

Maximum Gain and Stability Factor



Stability

0.47 @ 1.3GHz

MaxGain

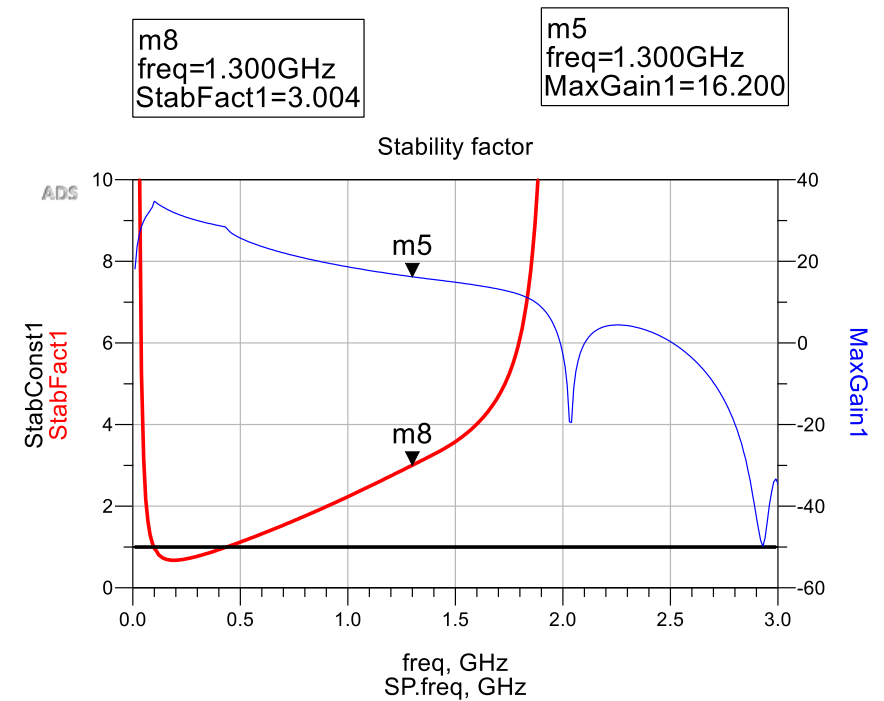
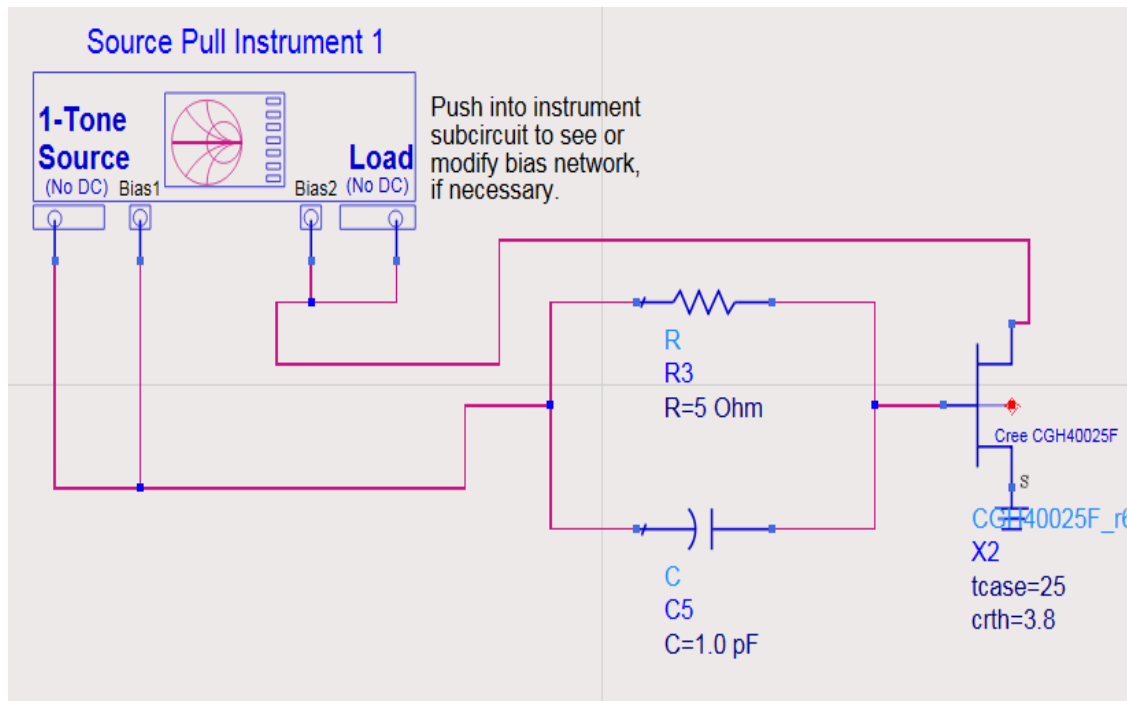
25 dB @ 1.3GHz

- Stability factor K tells us whether the device is unconditionally or conditionally stable
- MAXGain is the maximum Gain when the device is stable



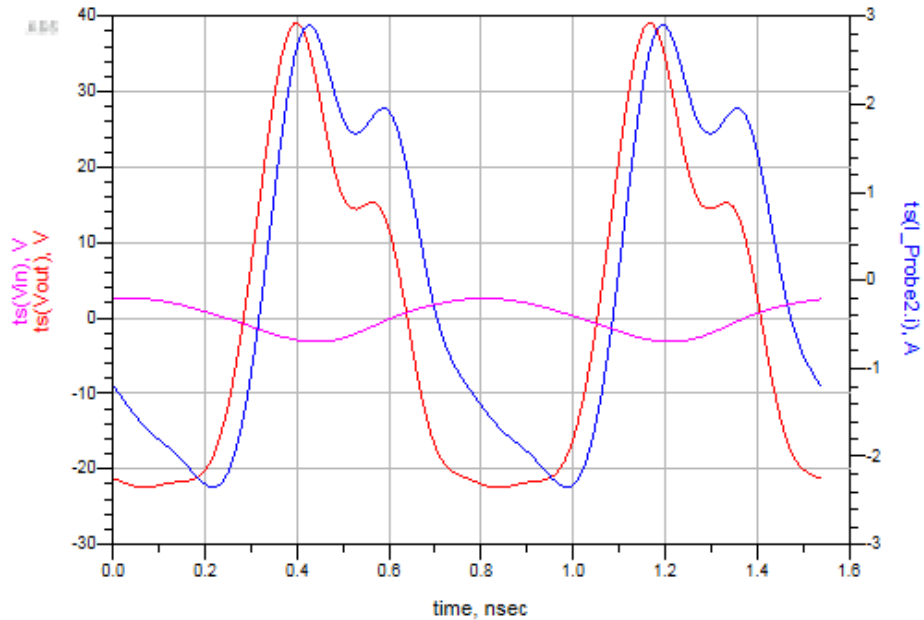
- Instability can overdrive and blow up the device
- Reduce Gain and power of the wanted signal
- Output Random interference

Stability (With stability network)

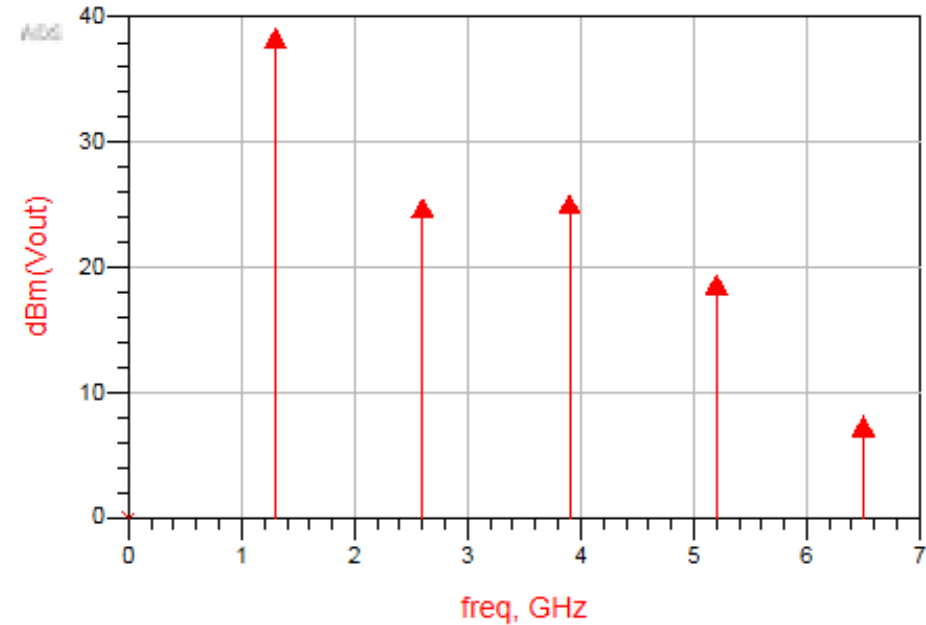


Harmonic Balance Simulation

Voltage and current output (time domain)

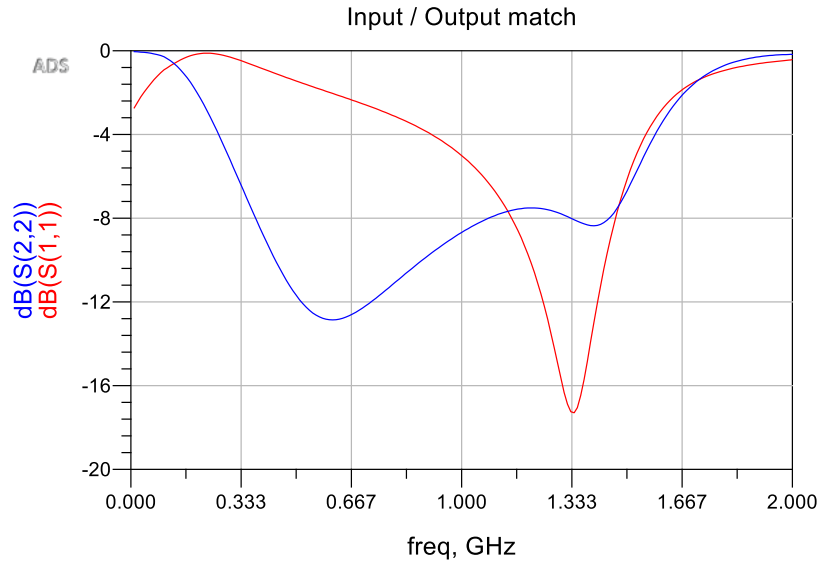
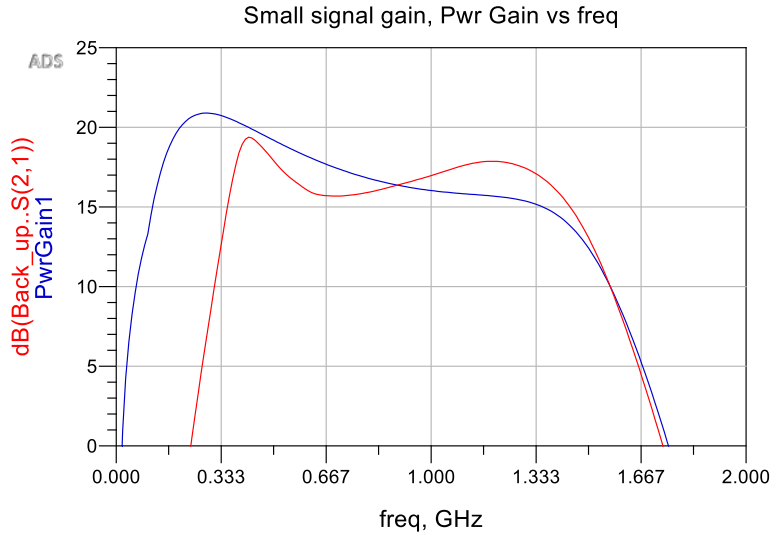
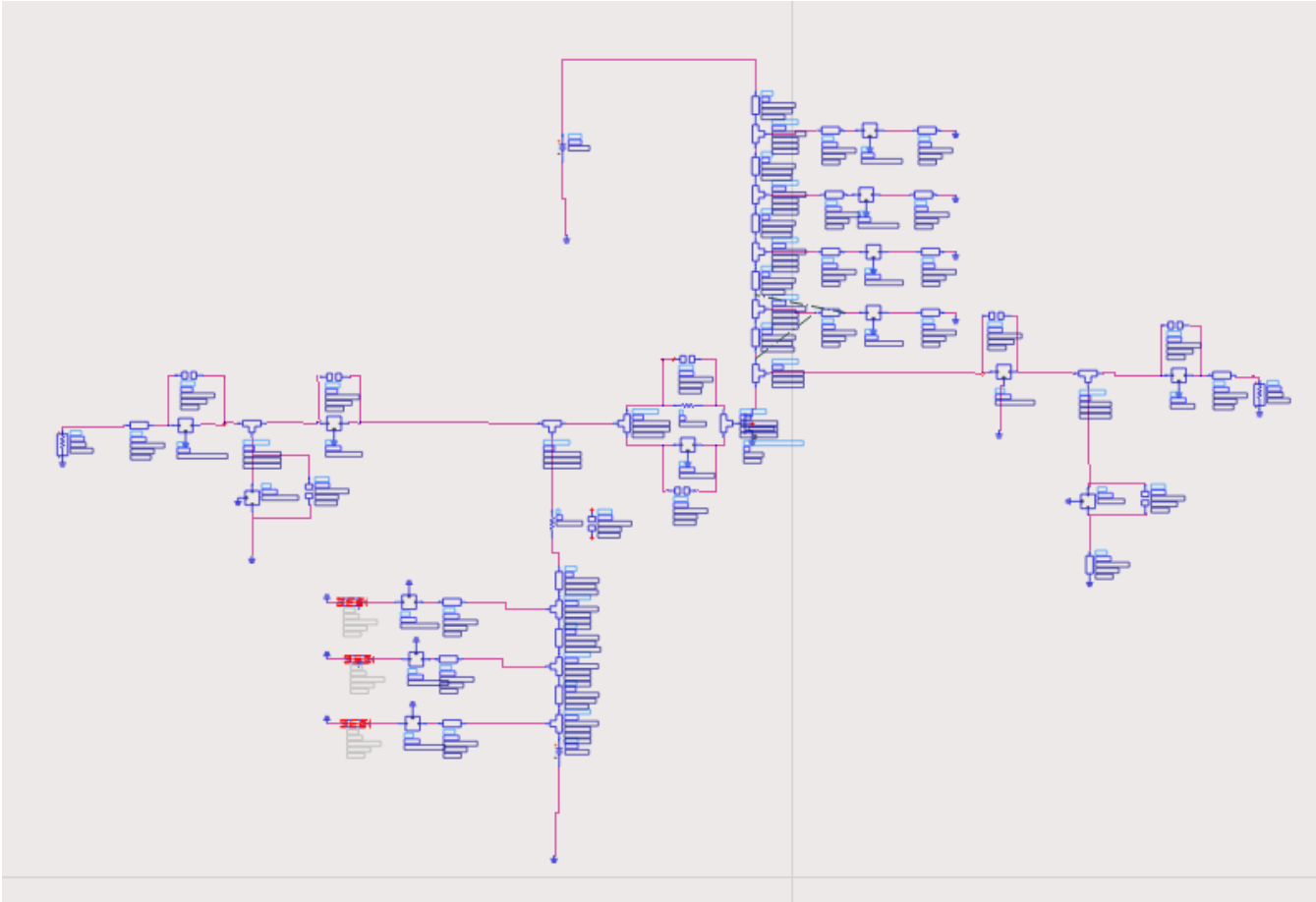


Voltage output (frequency domain)

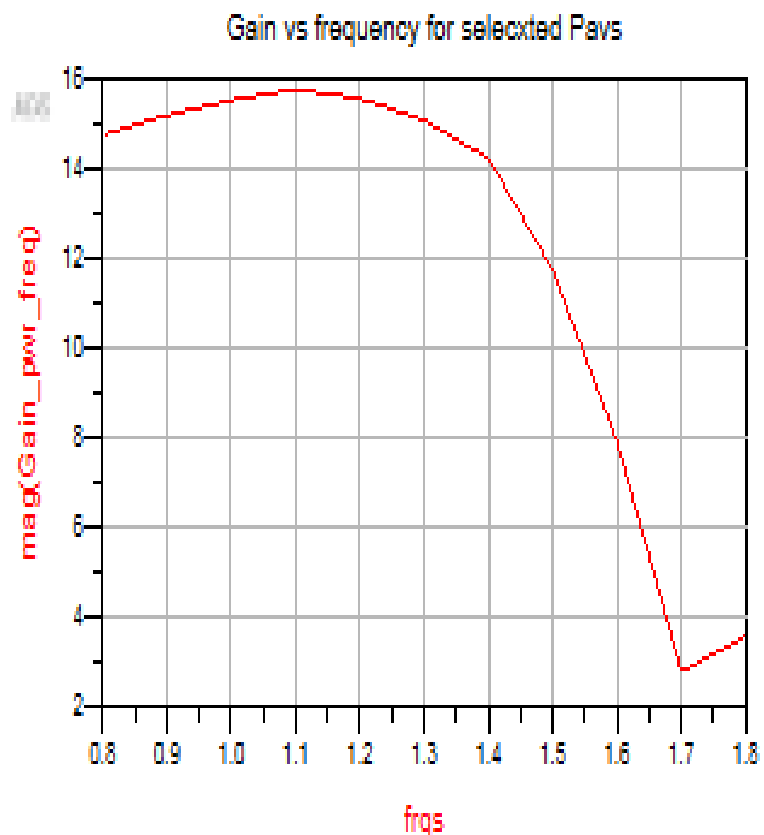
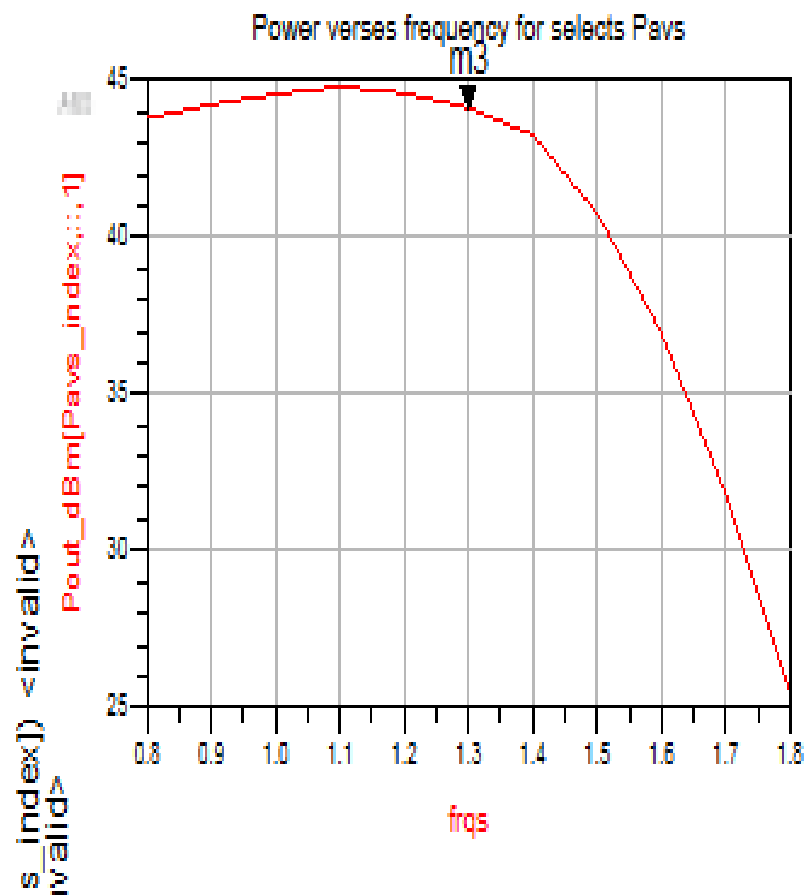


Pin (dBm)	Pout (dBm)	Gain (dBm)	Efficiency
30.4	45.4	15	67%

Final circuit



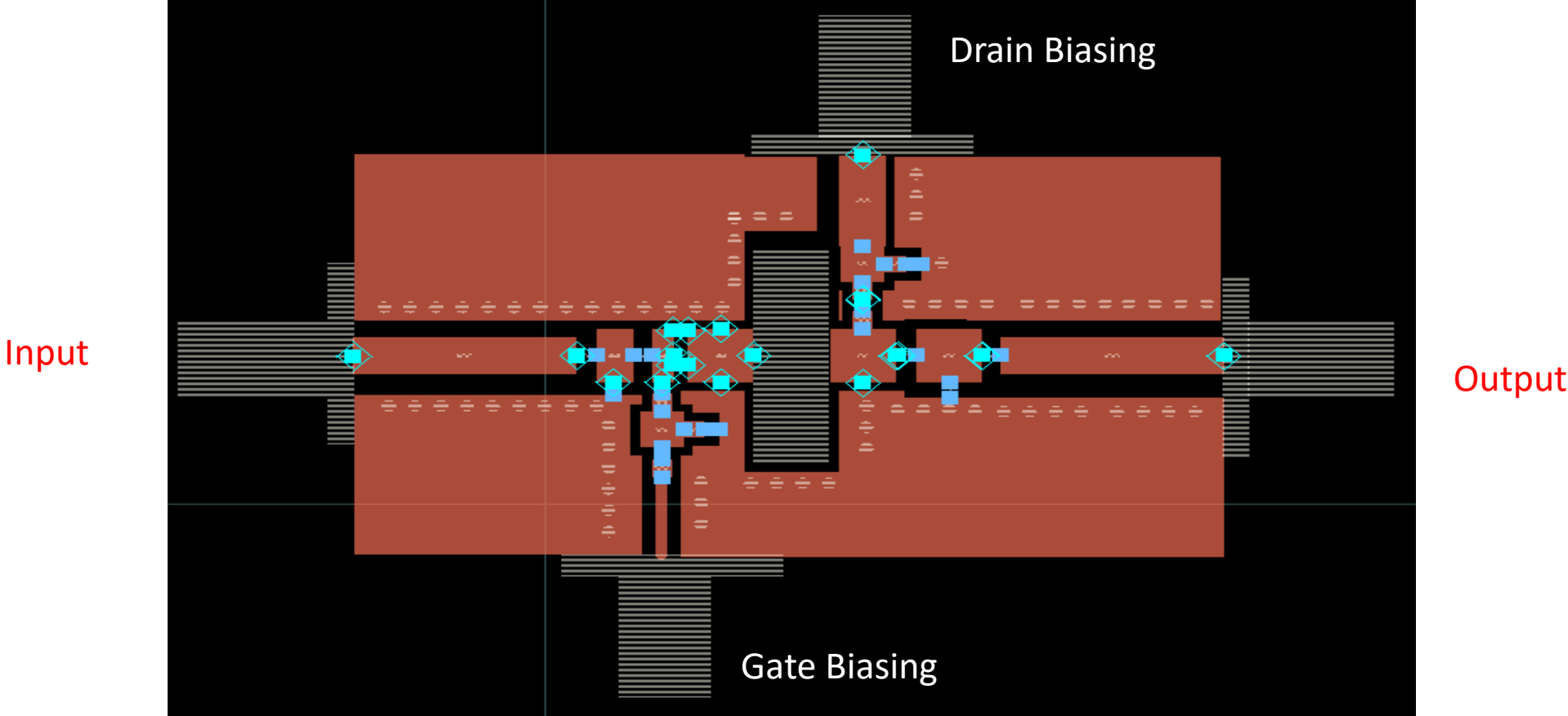
large Signal

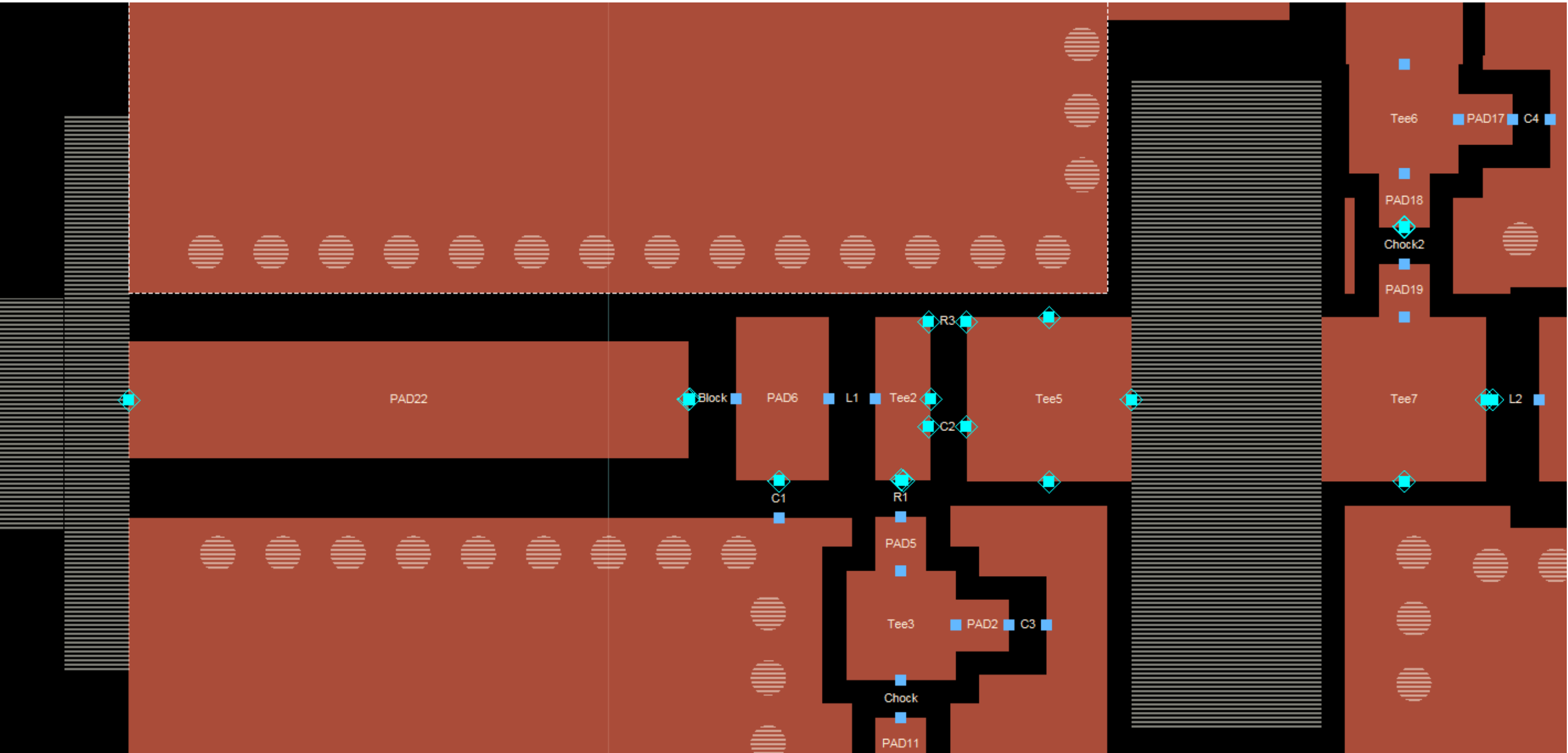


Power

Power Schematic	
Pout_W[Pavs_index,Frqs_index,1]	25.727 / 0.000
Power Equation	
Pcalc_dds[Pavs_index,Frqs_index,1]	25.727 / 0.000
Power dBm	
Pout_dBm[Pavs_index,Frqs_index,1]	44.104 / 0.000

PCB Layout Design





Immediate next step

- EM Simulation
- Get the PCB manufactured
- Build the circuit
- Final Test

